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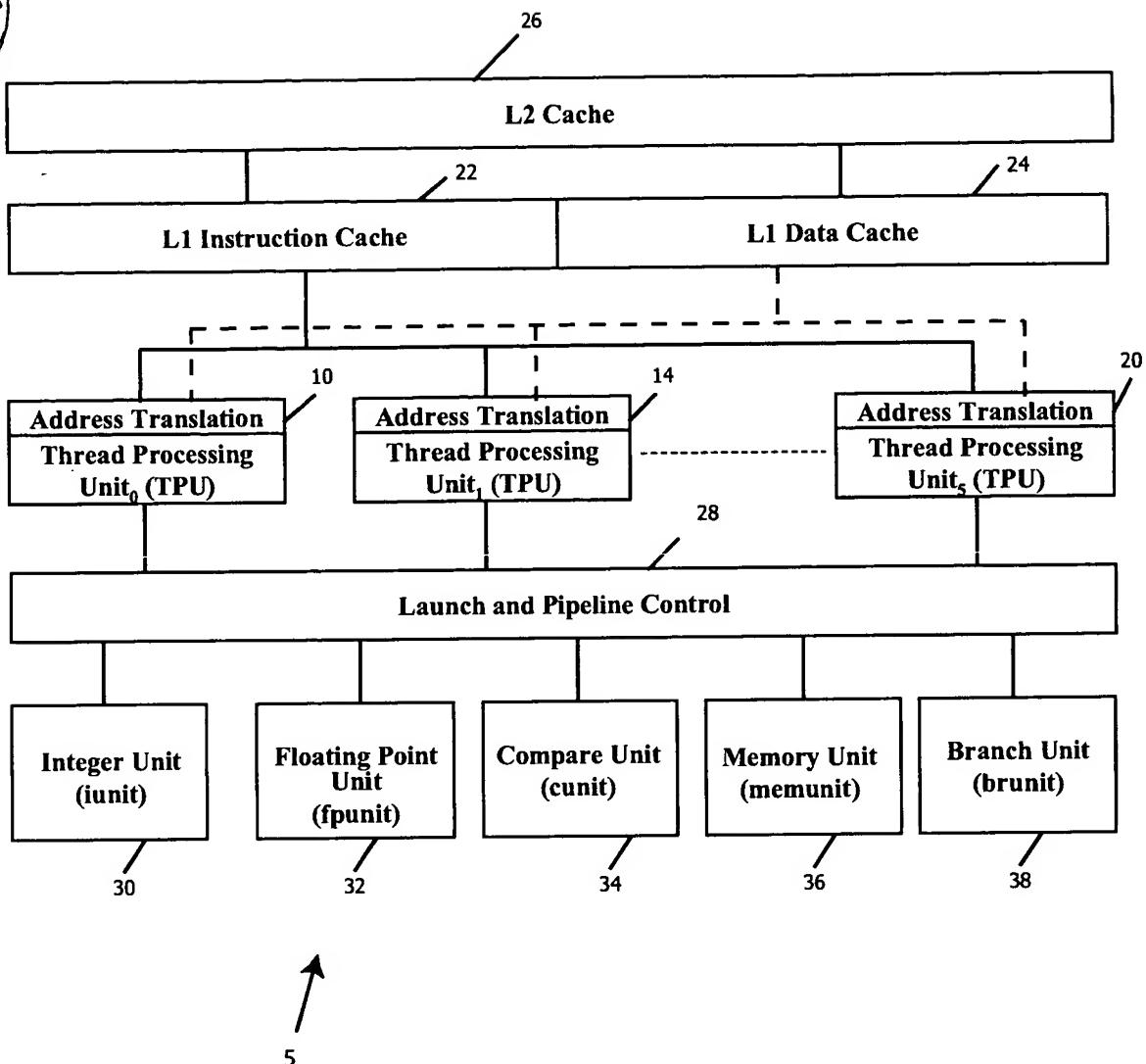


Figure 1

(Figures)

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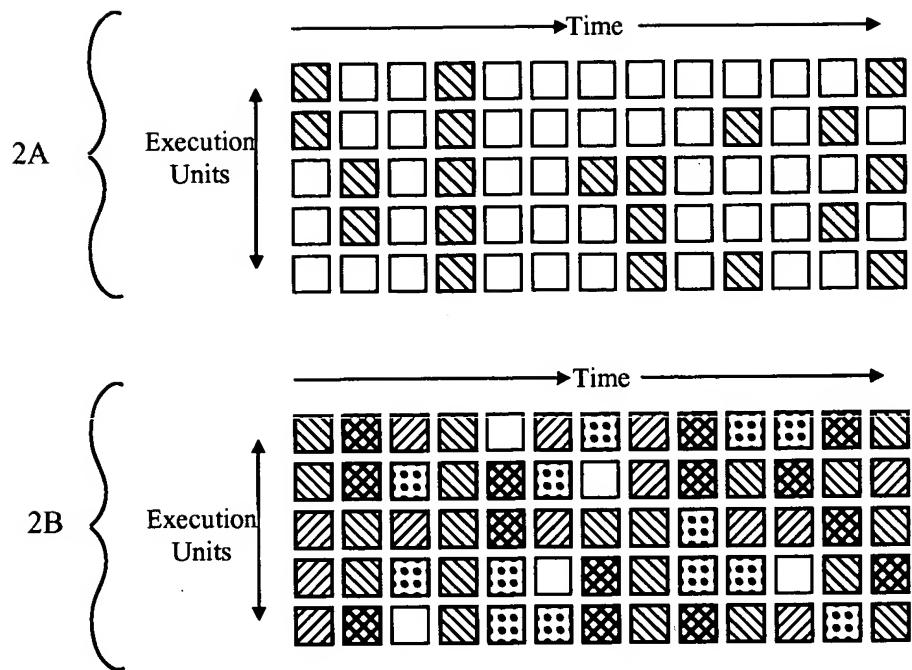


Figure 2

(Figures)

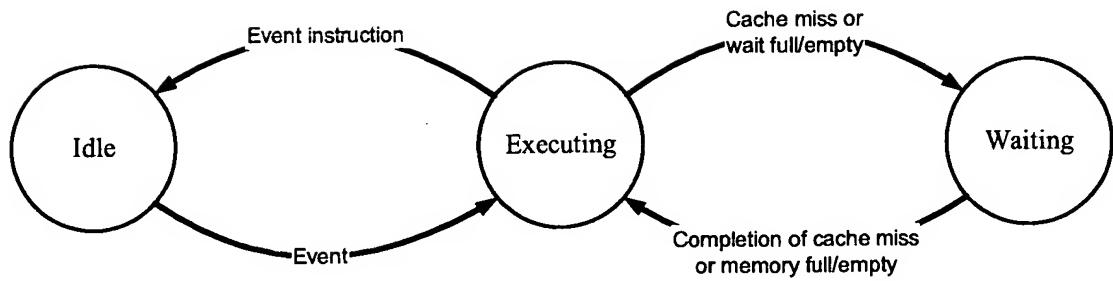


Figure 3

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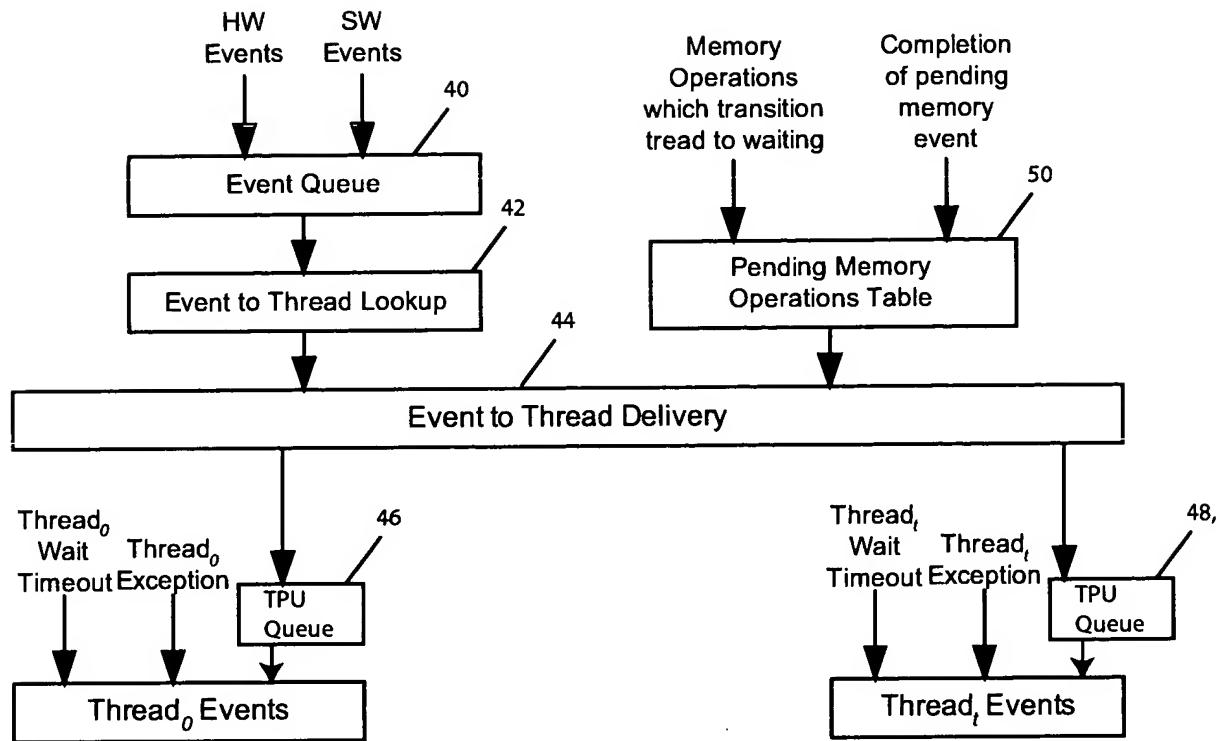


Figure 4

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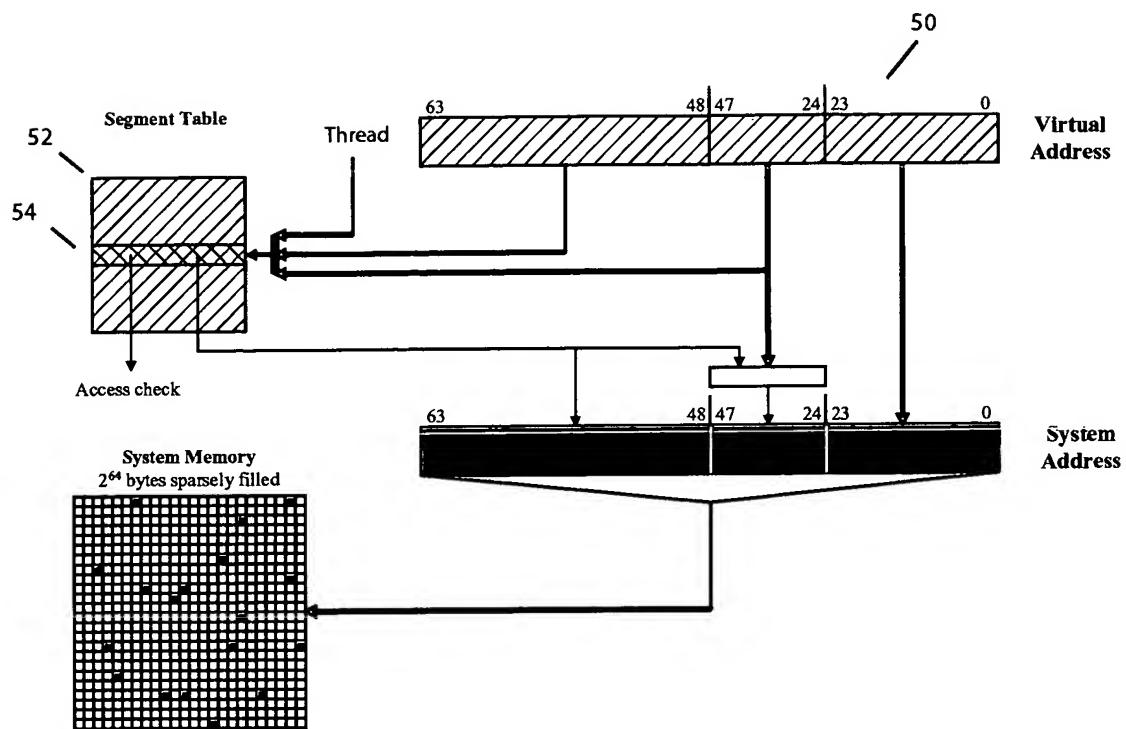


Figure 5

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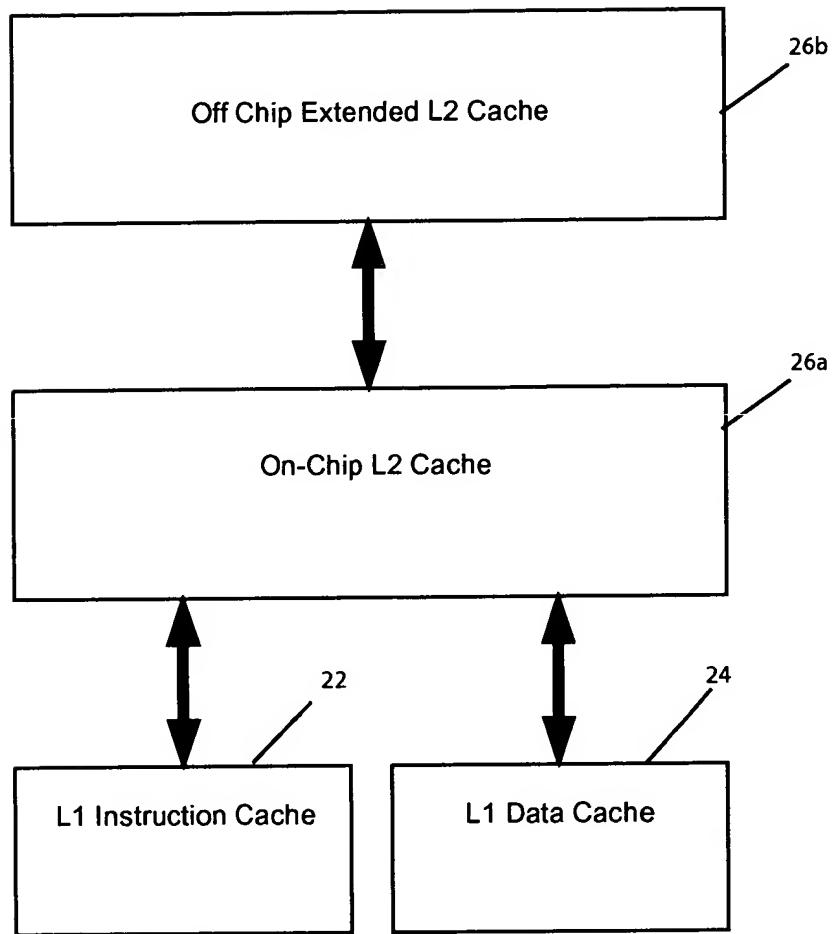


Figure 6

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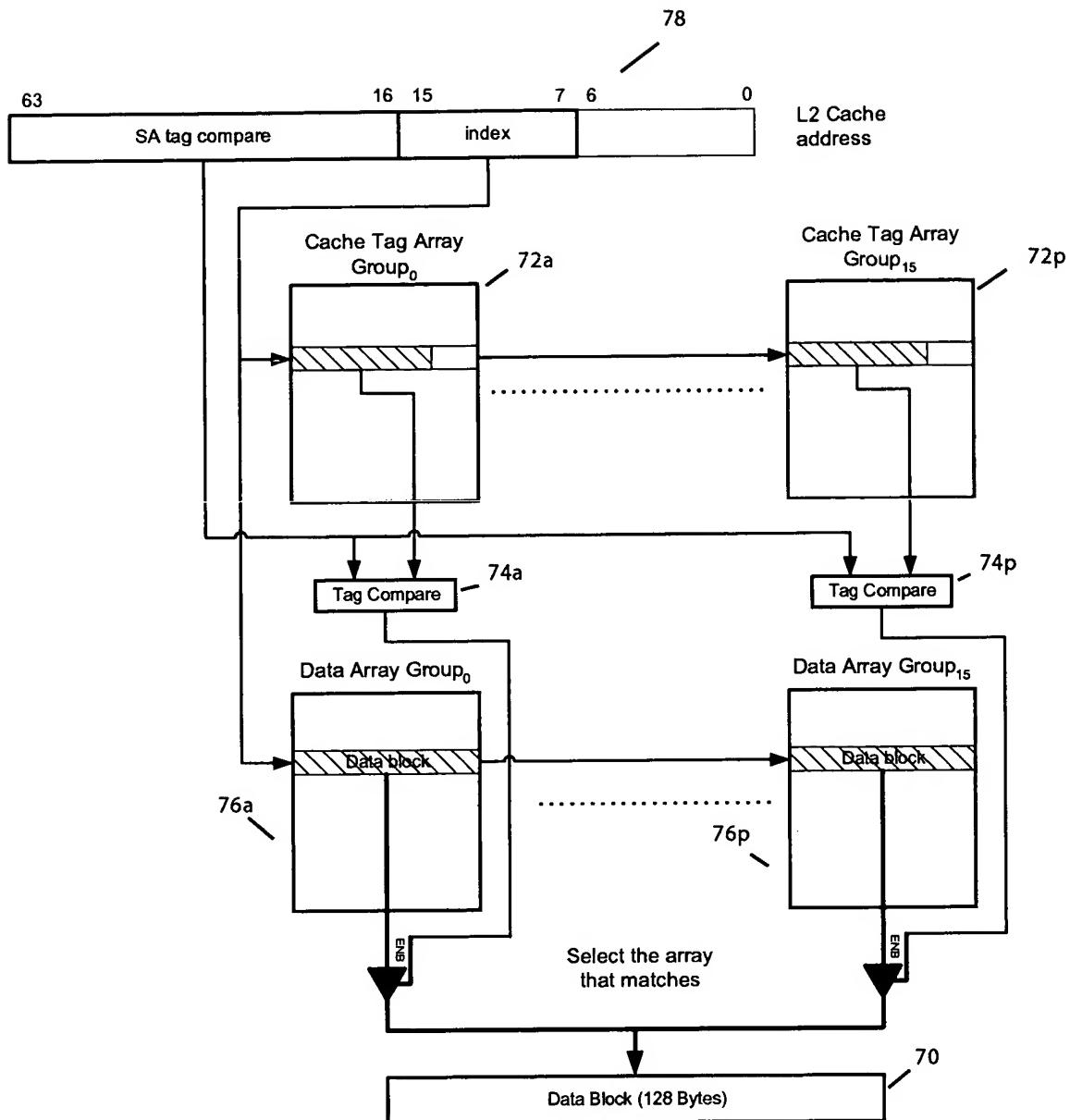


Figure 7

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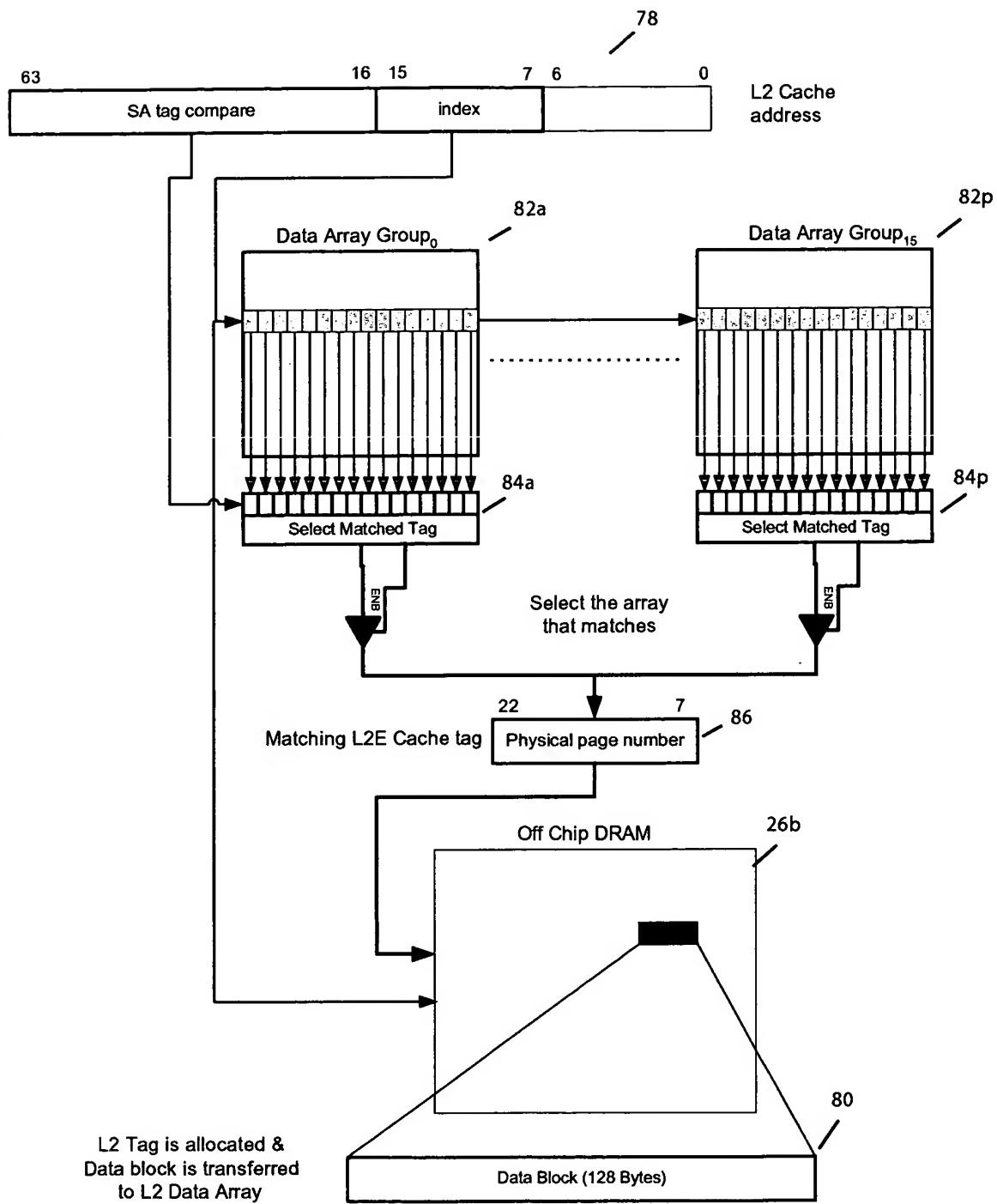
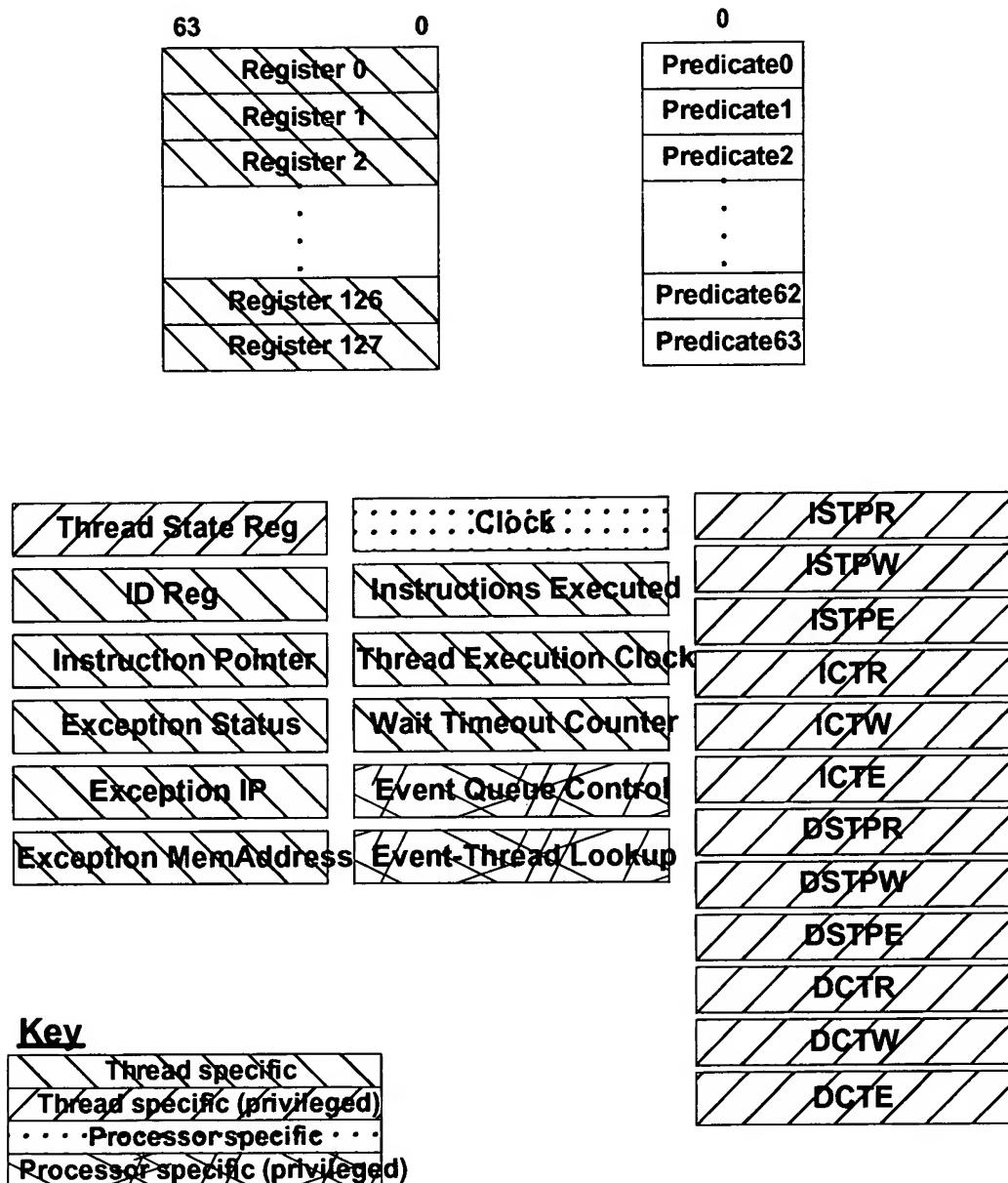


Figure 8

(Figures)



General Purpose Register File
TPU State Control Registers

Figure 9

(Figures)

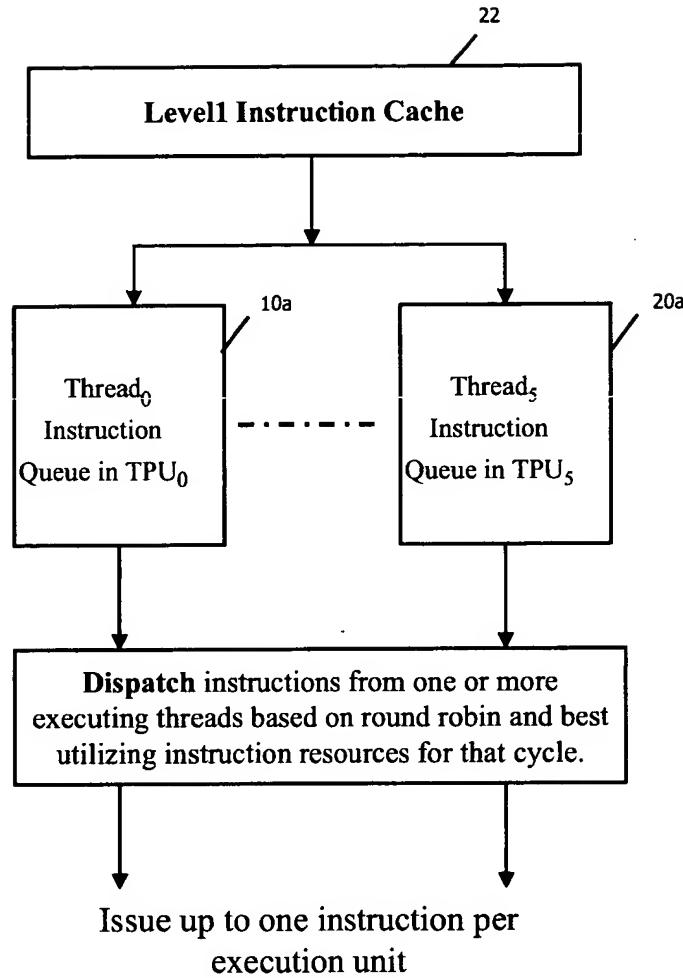


Figure 10

(Figures)



Logical Operation

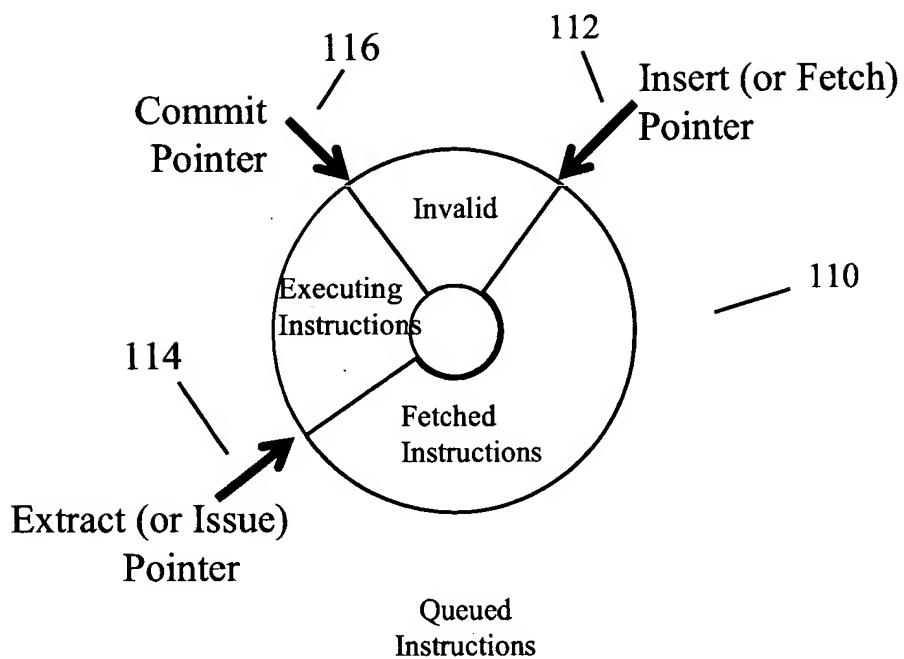


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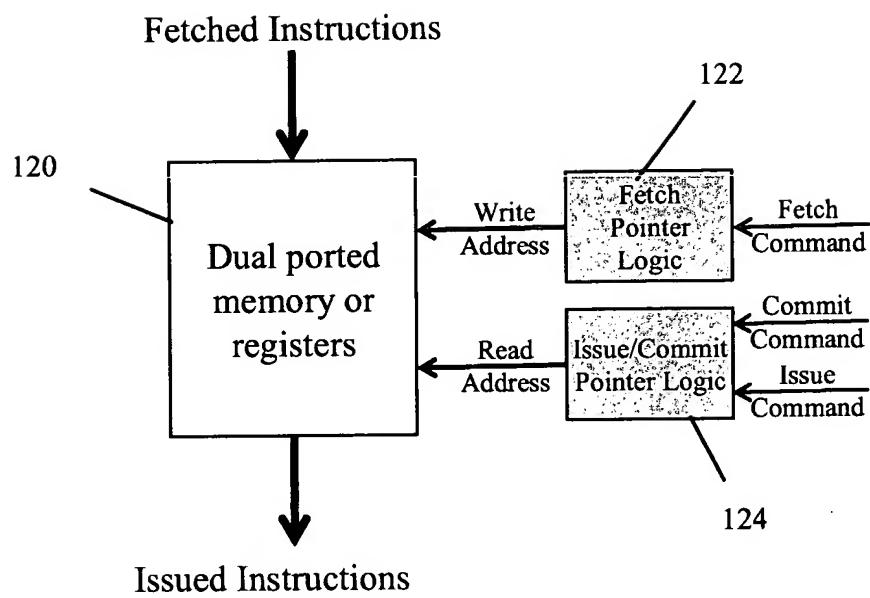


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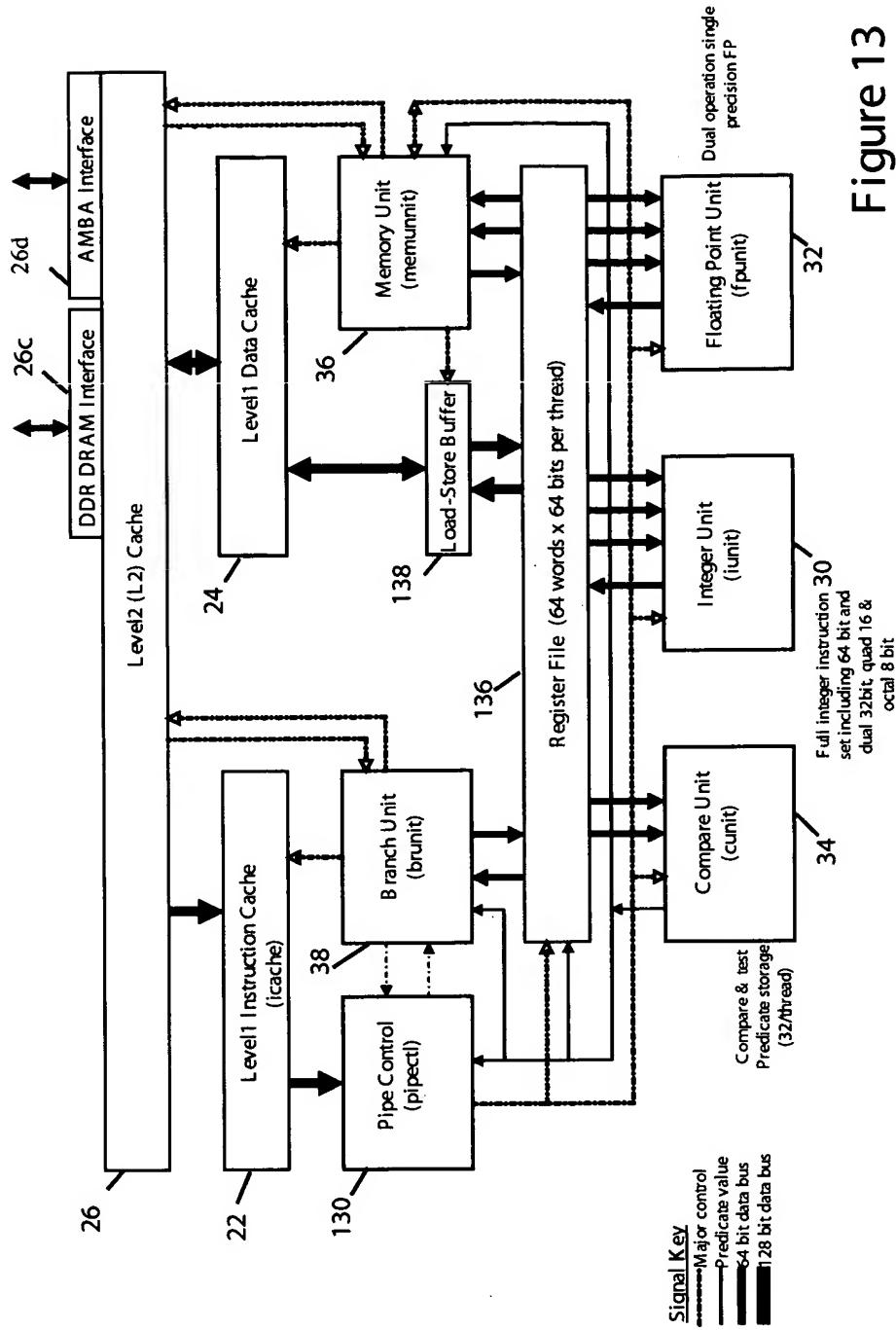


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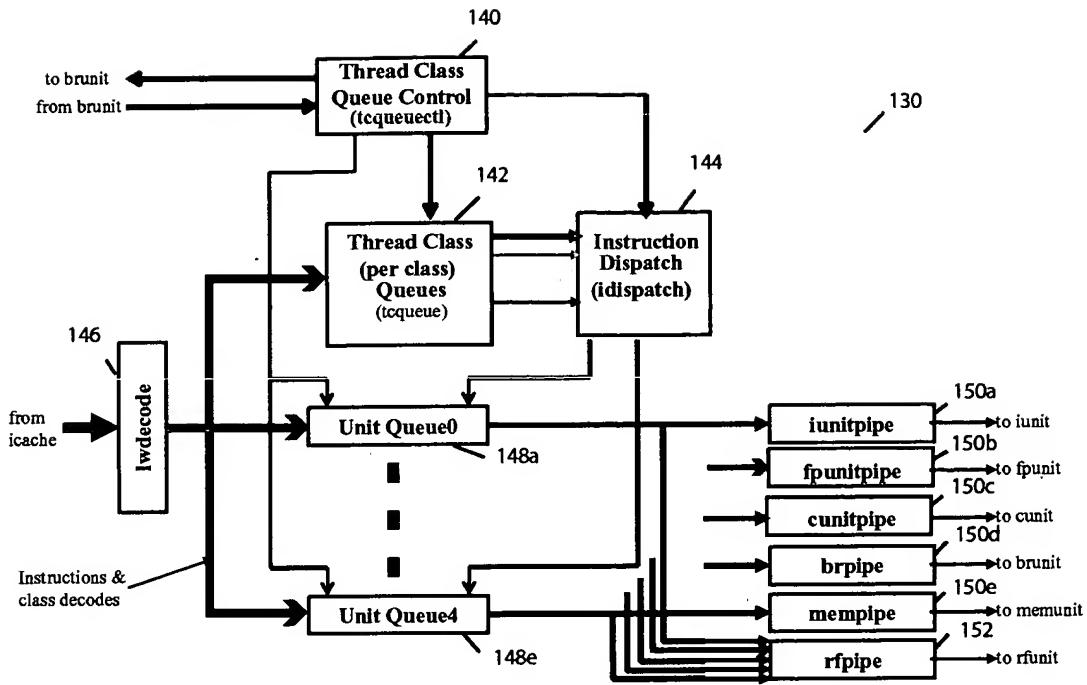


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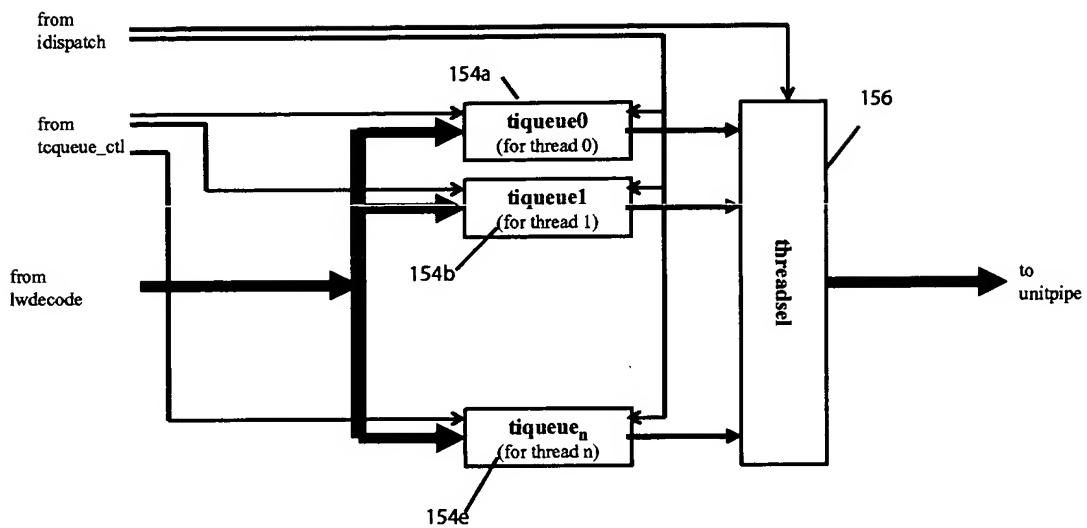


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38

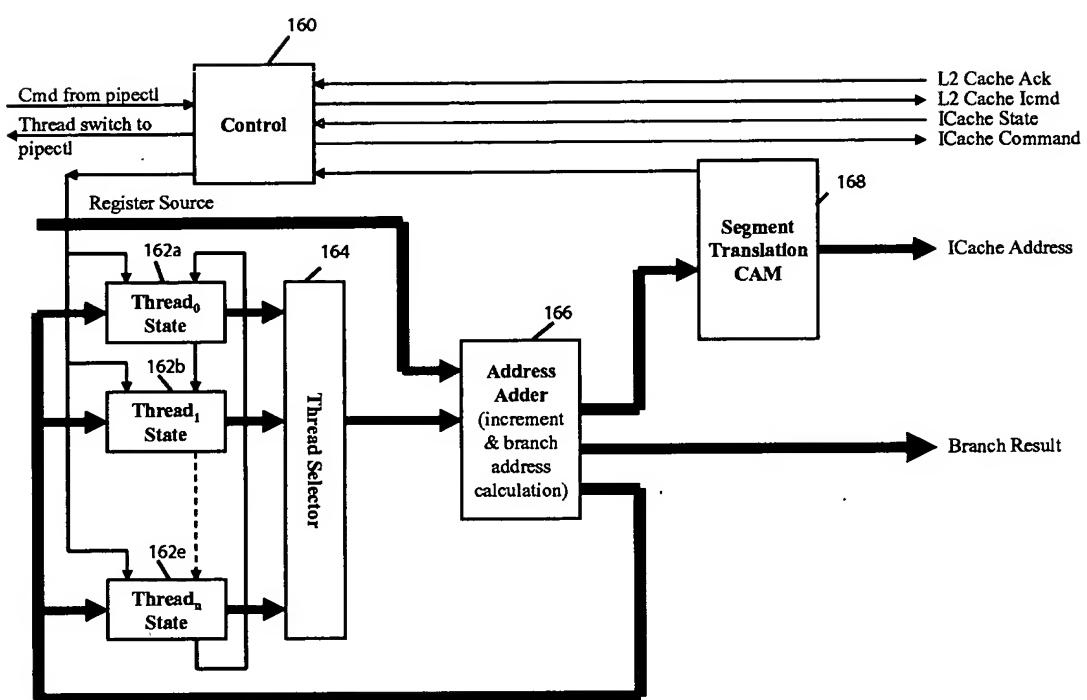


Figure 16

(Figures)



36

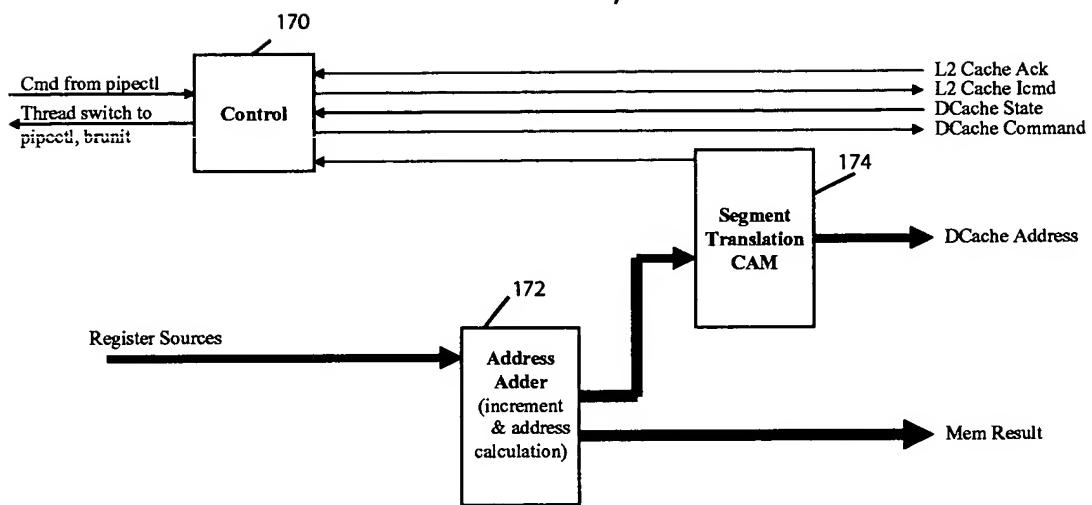


Figure 17

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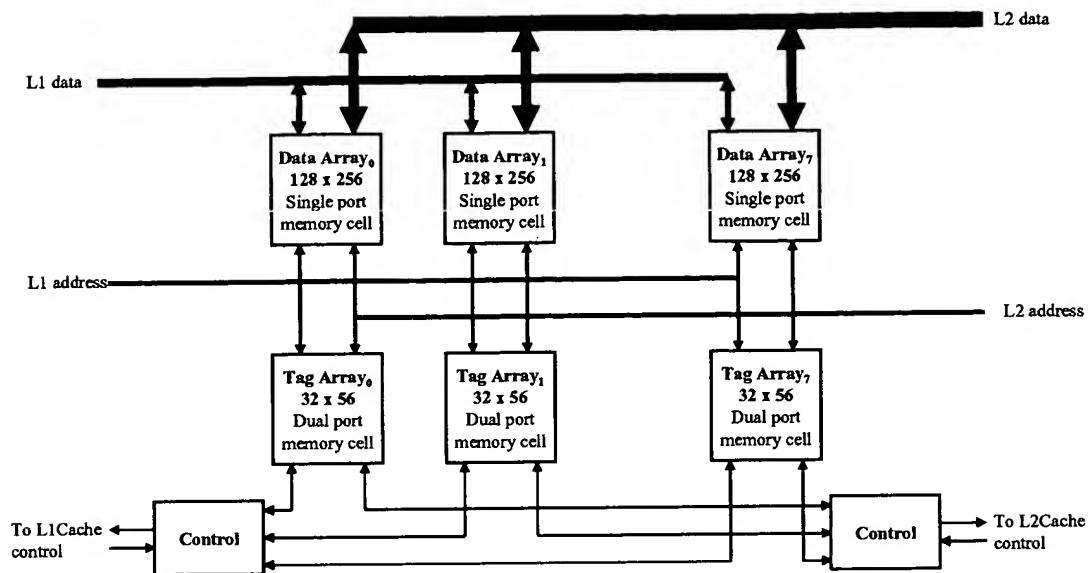


Figure 18

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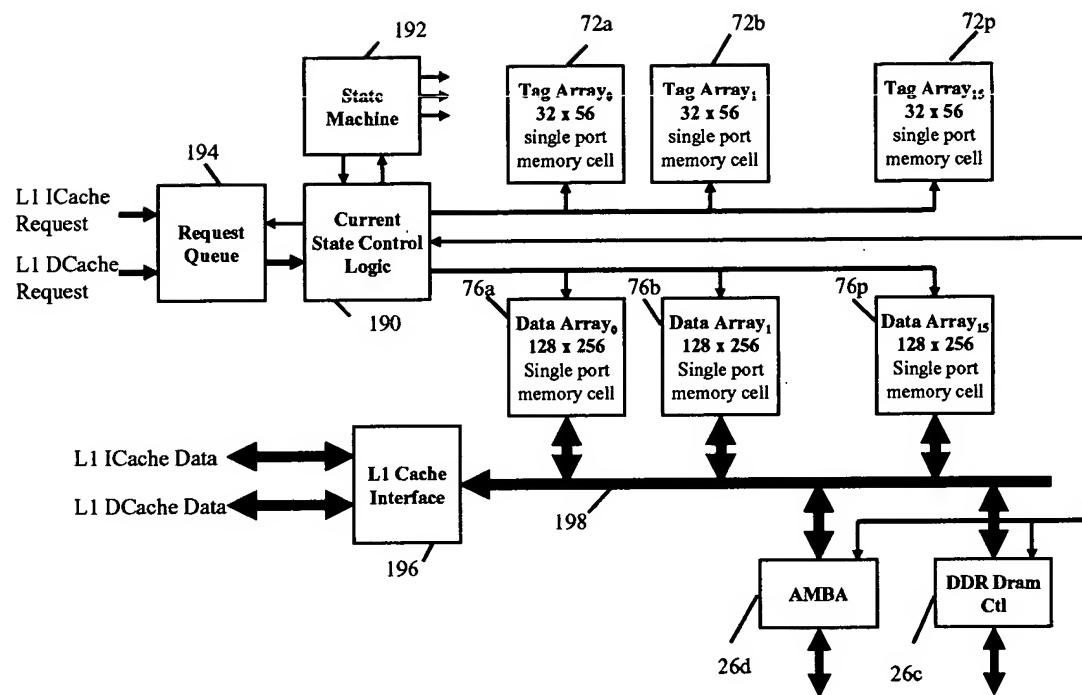


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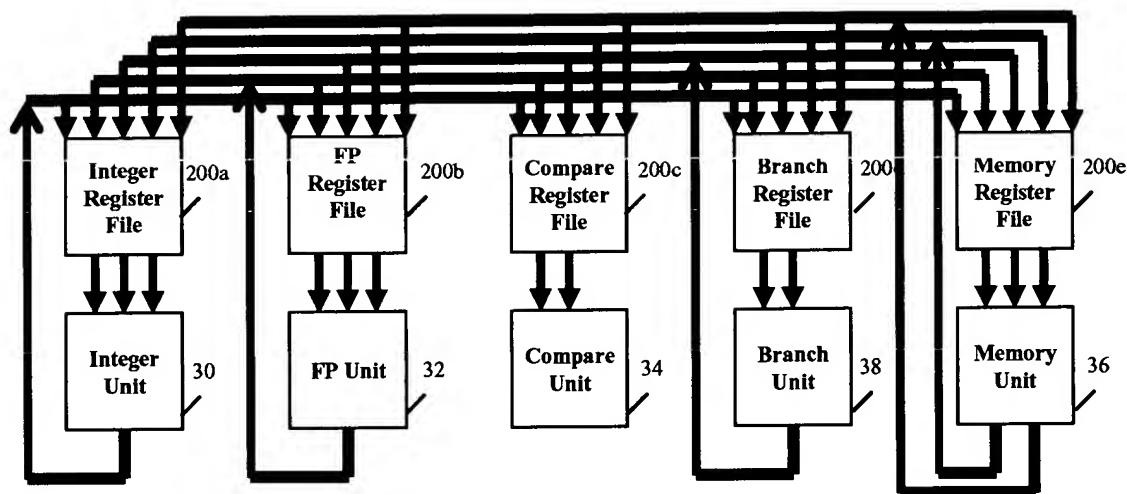


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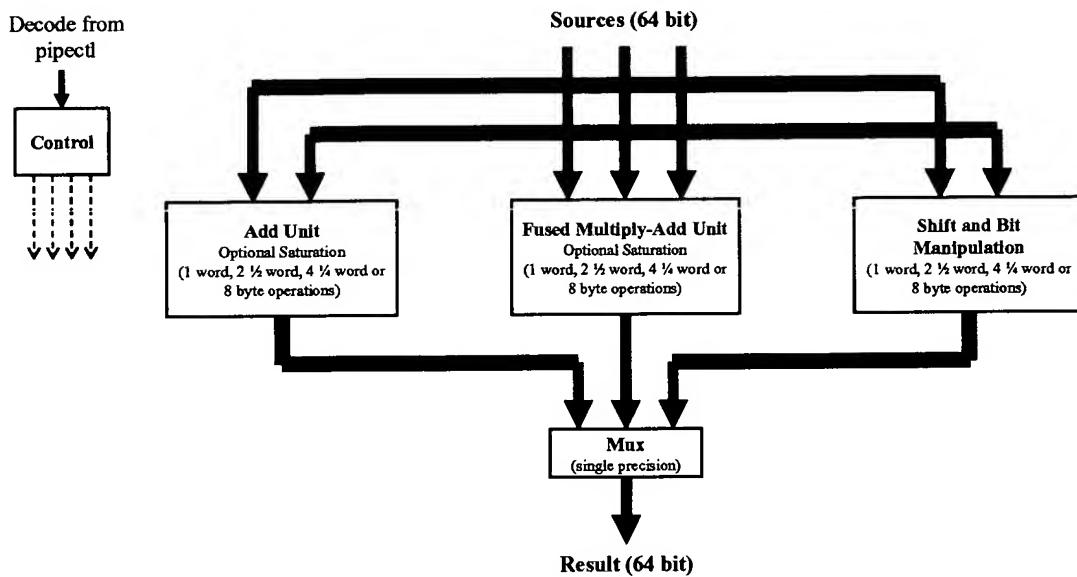


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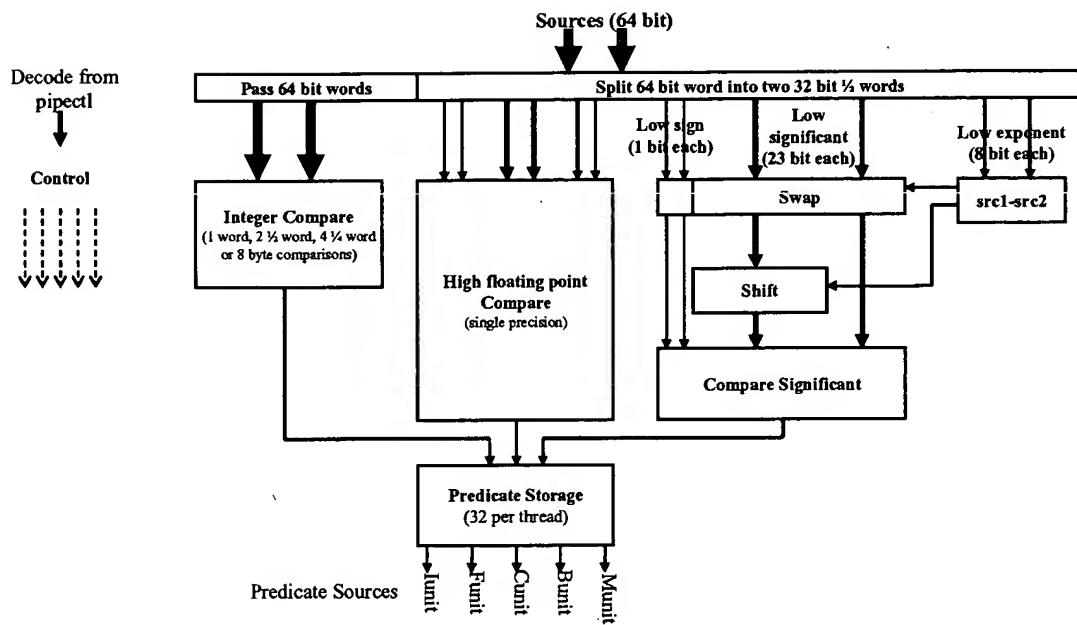


Figure 22

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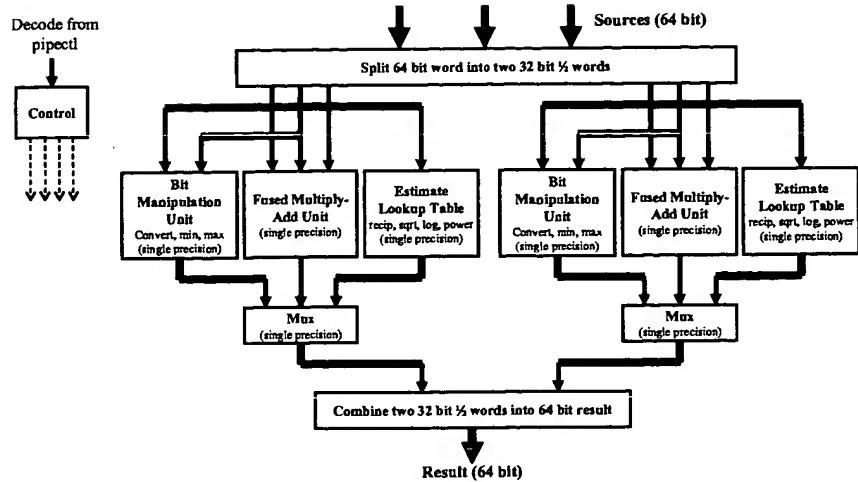


Figure 23A

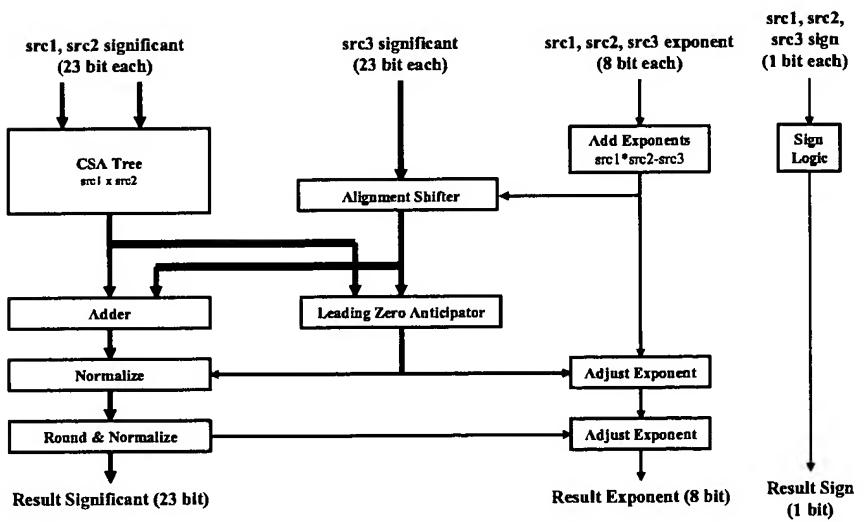


Figure 23B

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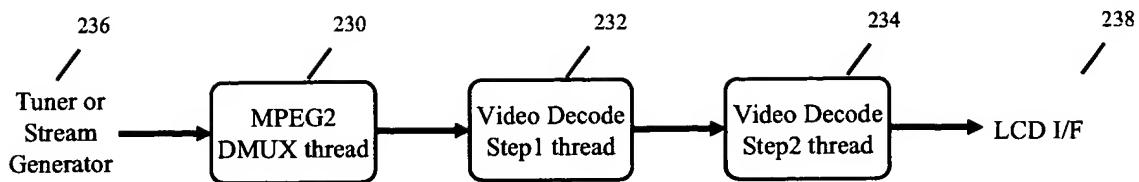


Figure 24A

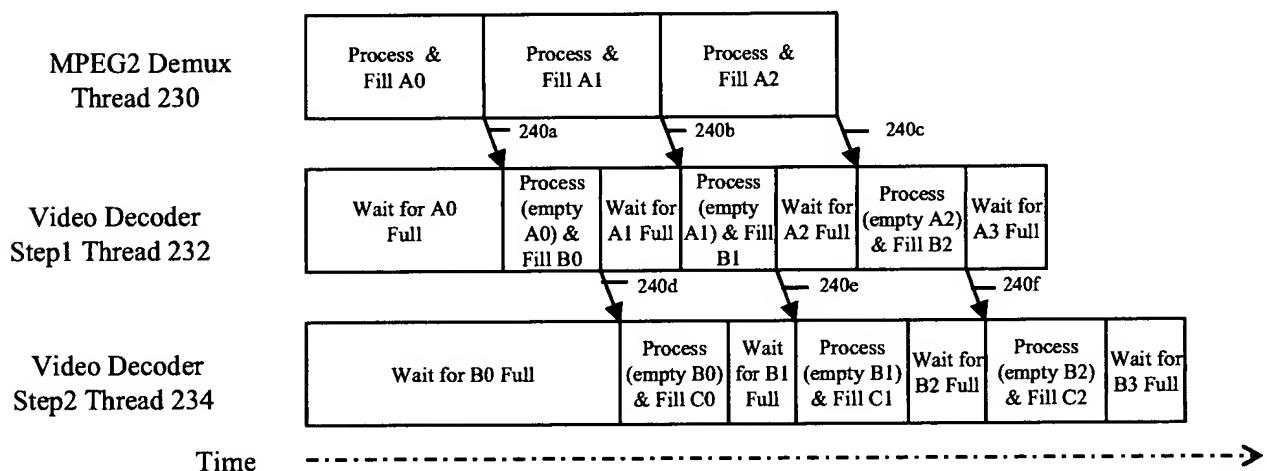


Figure 24B

(Figures)

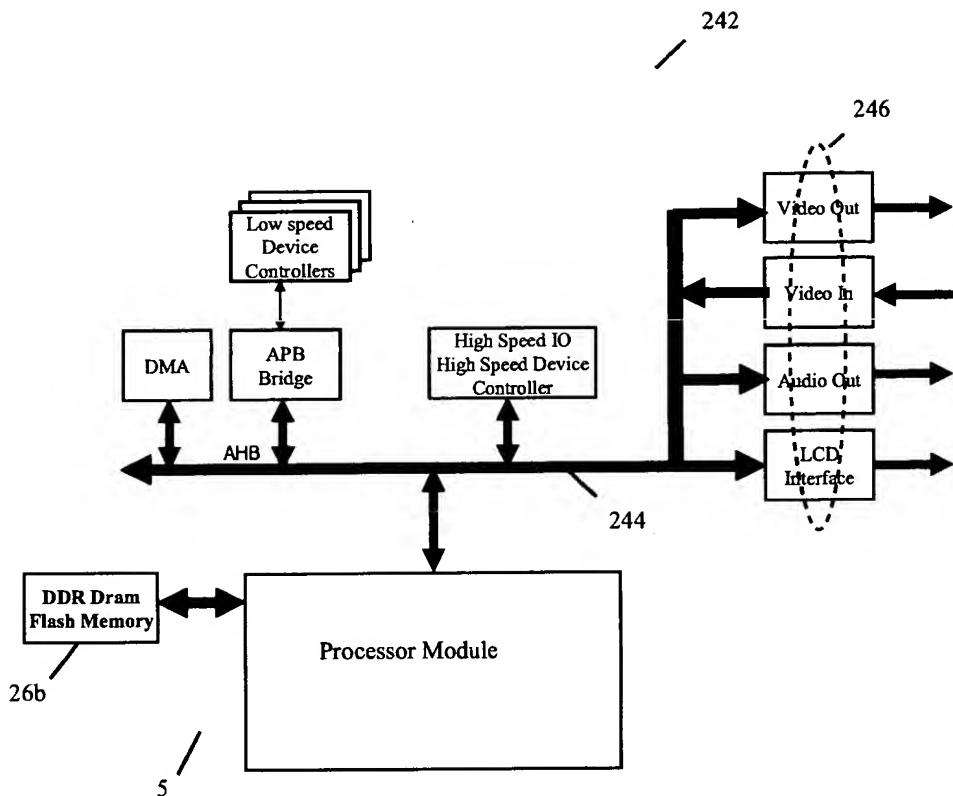


Figure 25

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SOC Block Diagram

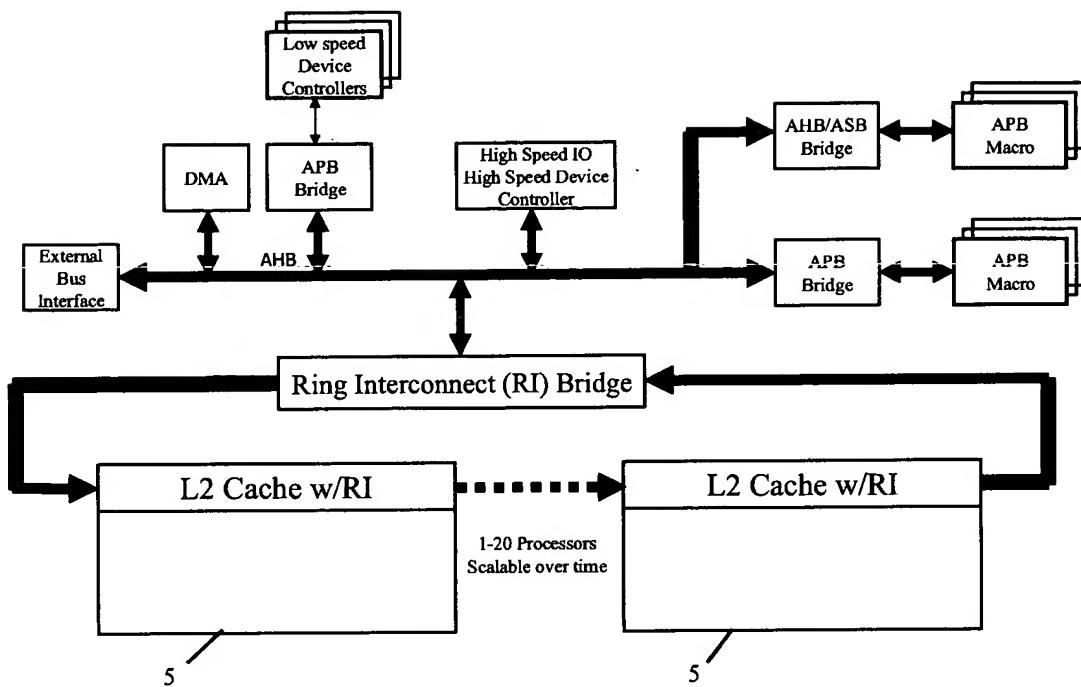


Figure 26

(Figures)